REMARKS

Summary Of The Office Action & Formalities

Claims 1-5 are all the claims pending in the application.

The Examiner has withdrawn the previous prior art rejections, but now rejects the claims as follows:

1. Claims 1 and 4 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Wong et al. in view of Cloonan et al. (US 5,642,349).

2. Claims 2, 3 and 5 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Wong et al. in view of Cloonan et al. and Petersen (USP 5,467,347).

Applicant respectfully traverses.

Claim Rejections - 35 U.S.C. § 103

1. Claims 1 And 4 In View Of Wong et al. and Cloonan et al.

As stated in the Manual Of Patent Examining Procedure ("MPEP"),

> To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

MPEP §2142. Applicant submits that the grounds of rejection do not meet these criteria. In particular, Wong et al. and Cloonan et al. when considered together, do not establish the requisite

suggestion or motivation to modify the switching architecture disclosed in Wong et al. in order to obtain the claimed invention. Furthermore, these references do not teach or suggest all the claim limitations.

In rejecting claims 1 and 4 in view of Wong et al. and Cloonan et al., the grounds of rejection acknowledge that Wong et al. does not "disclose an exclusive association between each inlet stage input/outlet stage output and each set of Q outputs/Q' inputs (r lines) such that the flow of data at each input of the inlet stage can be directed to each matrix of the outlet stage." Office Action at pages 3-4.

Indeed, as Applicant argued in its last response, Wong et al. does not teach that "each input . . . of the inlet stage can be connected to an output of the inlet stage which can be selected only from Q outputs . . . exclusively associated with that input; and in that each output . . . of the outlet stage can be connected to an input of the outlet stage which can be selected only from Q' inputs . . . of the outlet stage exclusively associated with that output." That is, nowhere does Wong et al. teach or suggest the exclusive relationship recited in claim 1 between each input of the inlet stage and the associated Q outputs. Again, referring to Fig. 2 of the present application, for example, outputs $213_{1,1}$ through $213_{1,N}$ of the first inlet stage matrix 211_1 are exclusively associated with inputs 212_1. Similarly, outputs $213_{R,1}$ through $213_{R,N}$ of the first inlet stage matrix 211_1 are exclusively associated with inputs 212_R.

Cloonan et al. does not make up for the above deficiency. Cloonan et al. discloses a ***very particular*** switching architecture that is complete from input to output. One skilled in the art would not understand this reference to make the sort of ***generalized*** teaching or suggestion

argued in the grounds of rejection that could have motivated the skilled artisan to modify the switching network in Wong et al. Rather, given the technology and the infinite possible variations for modifying a switching network, the skilled artisan would require explicit instructions as to how to go about modifying the network in Wong et al. in the manner asserted in the grounds of rejection. Otherwise, when faced with these two disclosures, the skilled artisan is likely to adopt ***one architecture or the other***, or engage in experimentation that could lead to any one of an infinite number of architectures.

Moreover, for the reasons set forth in Applicant's last response, Wong et al. would have ***taught away*** from Applicant's claimed invention, such that any experimentation, even in view of Cloonan et al., would lead the skilled artisan away from making the significant modifications needed to achieve the claimed invention. Applicant amended claim 1 to recite that the device for switching is "further configured so that the flow of data at each input of the inlet stage can be directed to each matrix of the outlet stage." Wong et al. clearly does not teach or suggest this feature. To the contrary, referring to Fig. 1 of the reference, if one assumes, for the sake of argument, that for a given first stage (n x m) matrix each input is exclusively associated with a particular group r of outputs, then clearly each of these inputs is <u>not</u> associated with <u>each</u> second stage (s x p) matrix. <u>The opposite is in fact illustrated in Fig. 1 of Wong et al.</u> Cloonan et al. does provide any direction to the skilled artisan to reject this feature of Wong et al. That is, the applied art provides no instruction on which features in Wong et al. and Cloonan et al. to reject and which to maintain, let alone how to combine features from these two references.

In short, the requisite teaching or suggestion for lifting certain features from one switching architecture and incorporating them into another switching architecture so as to achieve Applicant's claimed invention is simply not found in the applied art. Only when one skilled in the art relies on improper hindsight using Applicant's own disclosure as a road map can the skilled artisan reconstruct Applicant's invention.

Moreover, even if, for the sake of argument, one skilled in the art were to modify the switching architecture of Wong et al. in view of Cloonan et al., the resulting structure could not include all the features of Applicant's claims.

As a non-limiting example, contrary to the description provided in the grounds of rejection, Cloonan et al. does not disclose the feature wherein "each input . . . of the inlet stage can be connected to an output of the inlet stage which can be selected only from Q outputs . . . exclusively associated with that input . . . ." Referring to Fig. 4 of Cloonan et al., the input ports 17_0 to 17_{255} each fan out at a node to each of the pipes 18_0 to 18_3. Therefore, the input ports 17_0 to 17_{255} can be connected to all of the outputs at the node within the switching fabric 14A, and are not exclusively associated with a subset of these outputs. Furthermore, the architecture of each of the 16 x 16 matrices in $PIPE_0$ to $PIPE_3$ is not disclosed as one in which each input to the matrix is associated with an exclusive subset of outputs for that matrix. To the contrary, it appears that each input to the 16 x 16 matrix can be associated with all the outputs of that matrix. Therefore, even when combined, Wong et al. and Cloonan et al. fail to teach all the limitations of Applicant's claims.

In view of at least the foregoing distinctions, the Examiner is kindly requested to reconsider and withdraw the rejection of claim 1 and dependent claim 4. Additionally, regarding claim 4, Applicant continues to maintain that Wong simply lacks sufficient specificity to constitute anticipation of claim 4 for the reasons of record.

2. Claims 2, 3 And 5 In View Of Wong et al., Cloonan et al., And Petersen.

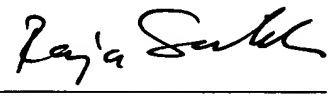
In rejecting claims 2, 3 and 5, the Examiner relies on Peterson for the same reasons set forth in the previous Office Action. Applicant maintains that, at best, the combination of Wong et al. Cloonan et al., and Petersen is an invitation to perform further research in switching architecture, but clearly lacks the specificity, including the disclosure of result-effective variables for constructing the switching devices of claims 2, 3, and 5.

Moreover, claims 2, 3 and 5 are believed to be allowable at least by reason of their respective dependencies.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



Raja Saliba
Registration No. 43,078

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

WASHINGTON OFFICE
23373
CUSTOMER NUMBER

Date: November 13, 2003